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Date of Deposit October 10, 2000

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MICHAEL BURNS

Docket No.: GR 98 P 1507

Date: October 10, 2000

Hon. Commissioner of Patents and Trademarks
Washington, D.C. 20231

S i r :

Enclosed herewith are the necessary papers for filing the following application for Letters Patent:

Applicant : ANDREAS RUSCH ET AL.

Title : SEMICONDUCTOR MEMORY DEVICE AND METHOD FOR FABRICATING IT

2 sheets of formal drawings in triplicate.
A check in the amount of $ 710.00 covering the filing fee.
PCT Publication (cover sheet only).

This application is being filed without a signed oath or declaration under the provisions of 37 CFR 1.53(d). Applicants await notification of the date by which the oath or declaration and the surcharge are due, pursuant to this rule.

The Patent and Trademark Office is hereby given authority to charge Deposit Account No. 12-1099 of Lerner and Greenberg, P.A. for any fees due or deficiencies of payments made for any purpose during the pendency of the above-identified application.

Respectfully submitted,

For Applicants

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GR 98 P 1507

SEMICONDUCTOR MEMORY DEVICE AND METHOD FOR FABRICATING IT

Cross-Reference to Related Application:

This is a continuation of copending International Application PCT/DE99/00901, filed March 25, 1999, which designated the United States.

Background of the Invention:

Field of the Invention:

The present invention relates to a semiconductor memory device and a method for fabricating it.

Although applicable, in principle, to any semiconductor memory devices, the present invention and the problems on which it is based will be explained with regard to ROM memories or read-only memories using silicon technology.

Known ROM semiconductor memory devices of this type use horizontal or vertical MOSFETs as semiconductor memory cells. A customary method for programming such ROM memories consists in modifying threshold voltages of the MOSFETs used in a ROM cell array in accordance with the desired ROM contents by

suitably masked vertical channel implantations. In other words, at least two types of MOSFETs are produced, a first type having a first threshold voltage (e.g. without channel implantation) and a second type having a second threshold voltage (e.g. with channel implantation). One type is assigned the logic "1" and the other type the logic "0". Programmed in this way, each transistor can store a single bit.

It is a constant aim in memory development to increase the storage density, that is to say the number of bits that can be stored per unit area or unit volume. One approach in this direction is the continual miniaturization of the structures involved, for example through read only memories (ROM) memories having folded trench structures.

A further approach is in modifying the semiconductor memory elements in such a way that they can each store more than one bit. This can be achieved for example by performing more than one type of channel implantation, with the result that one bit can be stored per memory cell for each channel implantation.

By way of example, four different threshold voltages, that is to say 2 bits per memory cell, can be generated by four

different channel implantations. The different threshold voltages can be distinguished by use of a suitable read-out circuit.

Summary of the Invention:

It is accordingly an object of the invention to provide a semiconductor memory device and a method for fabricating it that overcomes the above-mentioned disadvantages of the prior art methods and devices of this general type, whose semiconductor memory elements can store more than one bit.

With the foregoing and other objects in view there is provided, in accordance with the invention, a semiconductor memory device formed of a semiconductor substrate having a first conductivity type and a surface. An insulating layer is disposed on the semiconductor substrate. A matrix of semiconductor memory elements is disposed in the substrate. The semiconductor memory elements include a plurality of contact holes formed in the insulating layer. One contact hole is formed in the insulating layer for each of the semiconductor memory elements. A bit definition region is disposed in the semiconductor substrate underneath each of the

contact holes. A contact plug is disposed in each of the contact holes and is in electrical contact with the bit definition region. The bit definition region is configured such that a contact resistance between the semiconductor substrate and the contact plug defines a bit to be stored in a respective one of the semiconductor memory elements. The bit definition region in a first group of the semiconductor memory elements is a first implantation region disposed at the surface of the semiconductor substrate and has a dopant of the first conductivity type for decreasing the contact resistance. The bit definition region in a second group of the semiconductor memory elements is a second implantation region disposed at the surface of the semiconductor substrate and has a dopant of a second conductivity type for increasing the contact resistance. The bit definition region in a third group of the semiconductor memory elements corresponds to the semiconductor substrate. A further contact region is disposed in the semiconductor substrate outside of the bit definition region. An evaluation circuit is connected to and evaluates the contact resistance of the semiconductor memory elements.

The idea underlying the invention consists in configuring the respective bit definition region in such a way that it defines the contact resistance between the substrate region and the

contact plug region in accordance with the bit to be stored in the respective semiconductor memory element. In other words, the contact hole implantation mask is used for programming, the contact holes being provided with a varying contact resistance. The different resistances can then be assessed during read-out by a suitable evaluation circuit.

The semiconductor memory device according to the invention and the method for fabricating it according to the invention have the following advantages, inter alia, over the known solution approaches. It is possible to realize three-value logic per memory cell using only two implantations. Therefore, for example, three bits can be stored in two cells. This saves a mask plane in comparison with the above-described method that is customary for MOSFETs. The programming does not take place until late in the process after the contact hole etching, which permits a favorable turnaround time. In the case of applications relevant to security, such as e.g. in the smart card field, subsequent read-out by backward preparation is possible only with difficulty.

Finally, no additional steps are necessary in the process sequence because many known overall processes have contact hole implantations in order to reduce the resistance of the

contacts to diffusion region, to be precise particularly when titanium silicide or the like is not used. That makes the semiconductor memory device according to the invention and the method for fabricating it according to the invention highly cost-effective.

In accordance with one preferred development, the bit definition region is an implantation region that is located at the surface of the substrate region and serves for setting the contact resistance between the substrate region and the contact plug region. Thus, the contact resistance can be accurately set.

In accordance with a further preferred development, the bit definition region is an implantation region of a dopant of the first conductivity type. This corresponds to a doping on the surface region of the substrate, that is to say, to a decrease in the contact resistance.

In accordance with a further preferred development, the bit definition region is an implantation region of a dopant of a second conductivity type. This corresponds to a counterdoping of the surface region of the substrate, that is to say, to an increase in the contact resistance.

In accordance with a further preferred development, the bit definition region of the semiconductor memory elements corresponds to the substrate region. Thus, it is possible to establish a first state in accordance with a first bit without additional outlay.

In accordance with a further preferred development, the substrate has a further contact region located outside the bit definition region. The further contact region forms a terminal for a simple evaluation circuit, which is additionally connected to the contact plug region in order thus to determine the electrical resistance of the semiconductor memory element.

In accordance with a further preferred development, provision is made of an evaluation circuit device for evaluating the contact resistance of the respective semiconductor memory elements. As indicated above, the evaluation circuit may have a resistance measuring device, but may also operate capacitively or inductively.

With the foregoing and other objects in view there is further provided, in accordance with the invention, a method for

fabricating the semiconductor memory device. The method includes the steps of:

a) providing a semiconductor substrate having a first conductivity type;

b) providing an insulating layer on the semiconductor substrate;

c) forming a matrix of contact holes down to the semiconductor substrate in the insulating layer in accordance with respective semiconductor memory elements;

d) providing a surface region of the semiconductor substrate situated underneath each of the contact holes with a contact resistance in accordance with a bit to be stored in a respective semiconductor memory element as a bit definition region of the respective semiconductor memory element, the contact resistance formed by the steps of:

d1) performing a first implantation with a dopant of the first conductivity type into a first group of the contact holes with remaining ones of the contact holes being masked;

d2) performing a second implantation with a dopant of a second conductivity type into a second group of the contact holes with remaining ones of the contact holes being masked; and

d3) leaving the surface region of the semiconductor substrate situated underneath the respective contact holes in a substrate doping in a third group of contact holes;

e) providing contact plugs in the contact holes, the contact plugs being in electrical contact with the bit definition region; and

f) providing a further contact region located in the semiconductor substrate outside the bit definition region.

Other features which are considered as characteristic for the invention are set forth in the appended claims.

Although the invention is illustrated and described herein as embodied in a semiconductor memory device and a method for fabricating it, it is nevertheless not intended to be limited

to the details shown, since various modifications and structural changes may be made therein without departing from the spirit of the invention and within the scope and range of equivalents of the claims.

The construction and method of operation of the invention, however, together with additional objects and advantages thereof will be best understood from the following description of specific embodiments when read in connection with the accompanying drawings.

Brief Description of the Drawings:

Fig. 1 is a diagrammatic, sectional view of one fabrication step of a semiconductor memory element of a semiconductor memory device in accordance with an embodiment of the invention;

Fig. 2 is a sectional view of a further fabrication step of the semiconductor memory element of the semiconductor memory device in accordance with the embodiment; and

Fig. 3 is a block circuit diagram of the memory device connected to an evaluation circuit.

Description of the Preferred Embodiment:

In all the figures of the drawing, sub-features and integral parts that correspond to one another bear the same reference symbol in each case. Referring now to the figures of the drawing in detail and first, particularly, to Fig. 1 thereof, there is shown a semiconductor memory device 1 formed of a substrate 10, an insulating layer 20 disposed on the substrate 10, a contact hole 25 formed in the insulating layer 20, a bit definition region 30, and an implantation I.

The method for fabricating the semiconductor memory device 1 according to the invention in accordance with the embodiment proceeds as follows.

The substrate 10 having a first conductivity type (e.g. n-type silicon) is provided. In this case, the term substrate 10 is intended to be understood in the general sense, that is to say need not be the physical support but may also be an epitaxial layer situated thereon, a diffusion region provided therein, or the like.

Next, the insulating layer 20 is provided on the substrate 10, in which layer there is to be formed a matrix of contact holes

25 to the substrate 10 in accordance with respective semiconductor memory elements.

For programming the semiconductor memory elements thus defined, after the formation of the respective contact holes 25, that surface region of the substrate 10 which is situated underneath the contact holes 25 is provided with a respective contact resistance in accordance with a bit to be stored in the respective semiconductor memory element as bit definition region 30 of the relevant semiconductor memory element.

This is done as follows in the present example.

All the contact holes 25 are defined and etched free photolithographically. The first implantation I into a first group of the contact holes 25 is then performed using a dopant of the first conductivity type n.

A second implantation is then performed using a dopant of a second conductivity type p in a second group of the contact holes 25.

A third group of the contact holes 25 remains covered during both implantations, that is to say does not receive implantation.

There are, then, the following semiconductor memory cells with increasing contact resistance: a contact implantation like the underlying substrate (e.g. like diffusion implantation), no implantation and contact implantation opposite to the underlying substrate, Fig. 1 showing only the first case.

Thus, it is possible to program three bits per two memory cells. Application in a three-value logic circuit device (ternary system) is also conceivable.

Fig. 2 is a schematic illustration of a further fabrication step of the semiconductor memory element of the semiconductor memory device 1 in accordance with the embodiment of the present invention.

In Fig. 2, in addition to the reference symbols already introduced, a contact plug 40 is provided.

After the programming of the respective semiconductor memory elements, the contact plugs 40 are provided in the contact

holes 25, which are in electrical contact with the bit definition region 30.

The substrate 10 expediently has a strip-type conductor strip structure, e.g. polysilicon or diffusion strips, the strips each forming a second terminal of the memory cells on a top side of the substrate, which, in addition to the respective contact plug 40, forms a terminal for an evaluation circuit with a resistance measuring device.

Although the present invention has been described above using preferred exemplary embodiments, it is not restricted thereto but rather can be modified in diverse ways.

In particular, further implantations can be carried out in order to produce semiconductor memory elements that can store even more logic values. Thus, the present invention makes it possible to fabricate a cost-effective multilevel ROM by application of the contact hole implantation(s), present in any case, for programming.

Fig. 3 shows a block circuit diagram of the semiconductor memory device 1 having the evaluation circuit 2 connected to an array of the memory cells 3. A bus 4 connects the

evaluation circuit 2 to the memory cells 3 and the bus 4 is partially formed of the strip-type conductor strip structure running in the semiconductor substrate 10.

We claim:

1. A semiconductor memory device, comprising:

a semiconductor substrate having a first conductivity type and a surface;

an insulating layer disposed on said semiconductor substrate;

a matrix of semiconductor memory elements disposed in said substrate, said semiconductor memory elements including:

a plurality of contact holes formed in said insulating layer, one of said contact holes formed in said insulating layer for each of said semiconductor memory elements;

a bit definition region disposed in said semiconductor substrate underneath each of said contact holes;

a contact plug disposed in each of said contact holes and disposed in electrical contact with said bit definition region, said bit definition region configured such that a contact resistance between said semiconductor substrate and said contact plug defines a bit to be stored in a

respective one of said semiconductor memory elements, said bit definition region in a first group of said semiconductor memory elements is a first implantation region disposed at said surface of said semiconductor substrate and has a dopant of said first conductivity type for decreasing said contact resistance, said bit definition region in a second group of said semiconductor memory elements is a second implantation region disposed at said surface of said semiconductor substrate and has a dopant of a second conductivity type for increasing said contact resistance, and said bit definition region in a third group of said semiconductor memory elements corresponds to said semiconductor substrate;

a further contact region disposed in said semiconductor substrate outside of said bit definition region;

an evaluation circuit connected to and evaluating said contact resistance of said semiconductor memory elements.

2. A method for fabricating a semiconductor memory device, which comprises the steps of:

providing a semiconductor substrate having a first conductivity type;

providing an insulating layer on the semiconductor substrate;

forming a matrix of contact holes down to the semiconductor substrate in the insulating layer in accordance with respective semiconductor memory elements;

providing a surface region of the semiconductor substrate situated underneath each of the contact holes with a contact resistance in accordance with a bit to be stored in a respective semiconductor memory element as a bit definition region of the respective semiconductor memory element, the contact resistance formed by the steps of:

performing a first implantation with a dopant of the first conductivity type into a first group of the contact holes with remaining ones of the contact holes being masked;

performing a second implantation with a dopant of a second conductivity type into a second group of the

contact holes with remaining ones of the contact holes being masked; and

leaving the surface region of the semiconductor substrate situated underneath the respective contact holes in a substrate doping in a third group of contact holes;

providing contact plugs in the contact holes, the contact plugs being in electrical contact with the bit definition region; and

providing a further contact region located in the semiconductor substrate outside the bit definition region.

Abstract of the Disclosure:

A semiconductor memory device is described that is formed of a semiconductor substrate. An insulating layer is disposed on the semiconductor substrate. A matrix of semiconductor memory elements is disposed in the substrate. The semiconductor memory elements include a plurality of contact holes formed in the insulating layer. One contact hole is formed in the insulating layer for each of the semiconductor memory elements. A bit definition region is disposed in the semiconductor substrate underneath each of the contact holes. A contact plug is disposed in each of the contact holes and is in electrical contact with the bit definition region. The bit definition region is configured such that a contact resistance between the semiconductor substrate and the contact plug defines a bit to be stored in the semiconductor memory elements. An evaluation circuit is connected to and evaluates the contact resistance of the semiconductor memory elements.

REL/bb

FIG 1

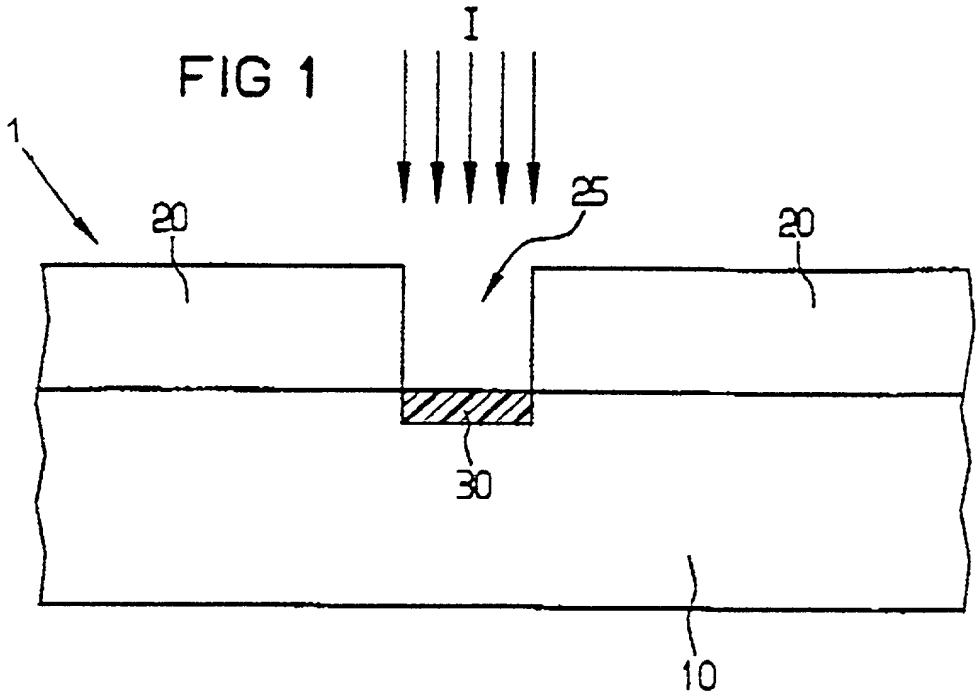
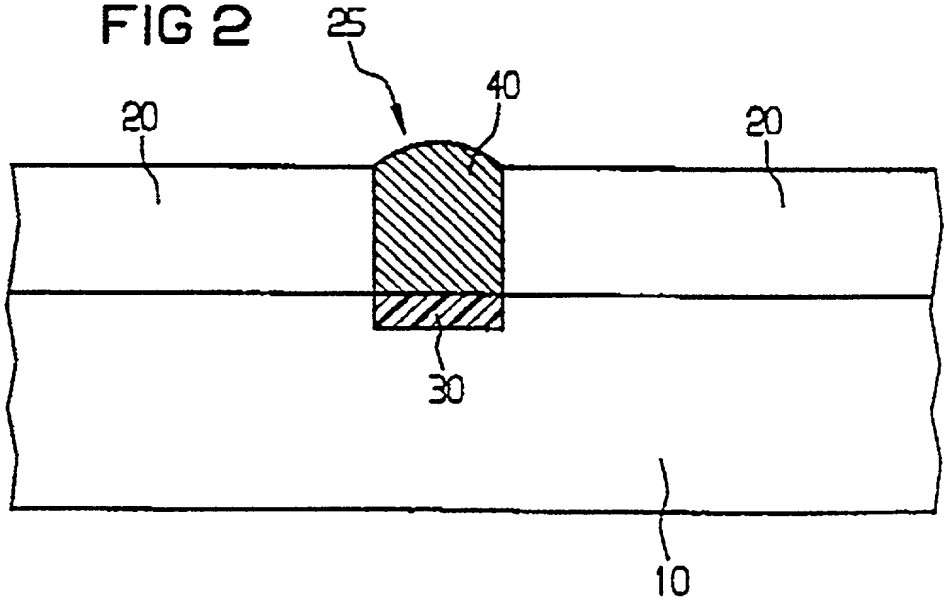


FIG 2



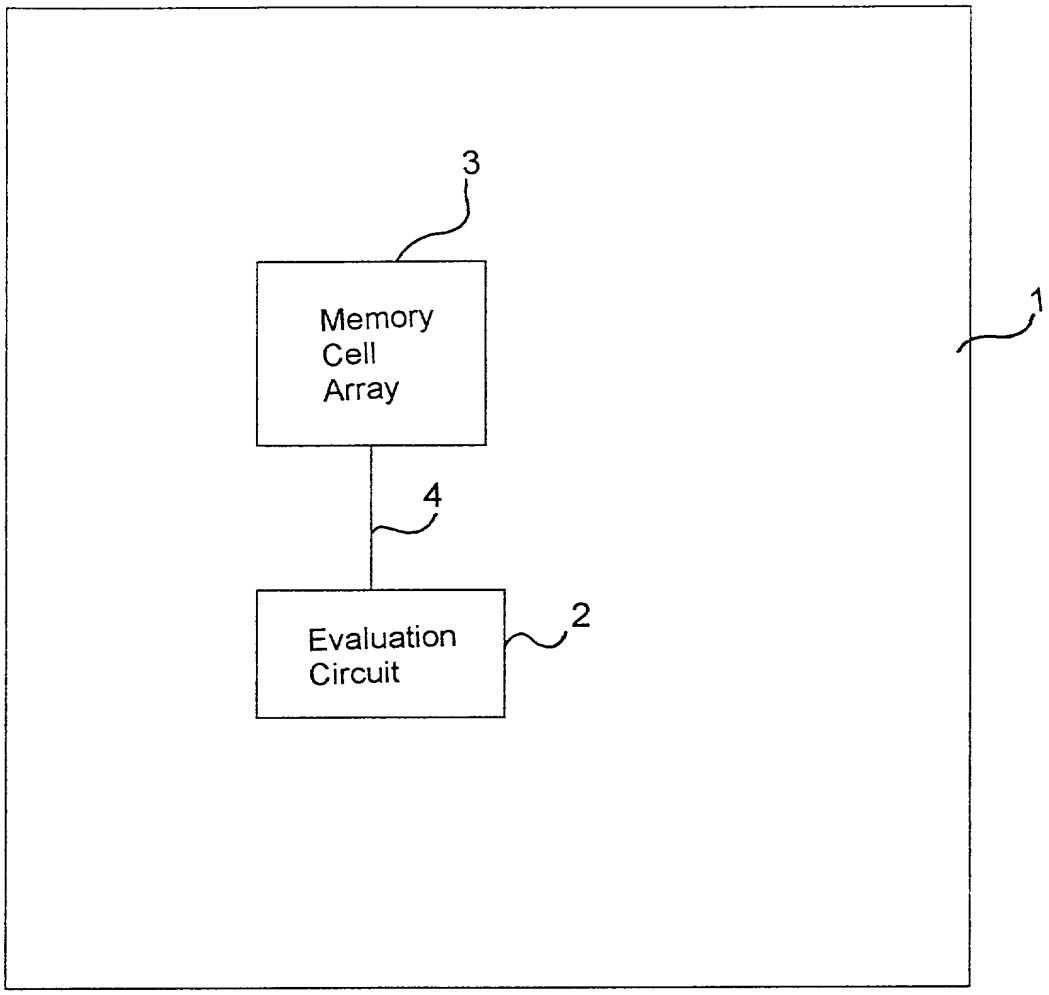


FIG 3

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COMBINED DECLARATION AND POWER OF ATTORNEY
IN ORIGINAL APPLICATION

As a below named inventor, I hereby declare that: my residence, post office address and citizenship are as stated below next to my name; that I verily believe that I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

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described and claimed in the specification bearing that title, that I understand the content of the specification, that I do not know and do not believe the same was ever known or used in the United States of America before my or our invention thereof, or patented or described in any printed publication in any country before my or our invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve month prior to this application, that I acknowledge my duty to disclose information of which I am aware which is material to the examination of this application under 37 C.F.R. 1.56a, and that no application for patent or inventor's certificate of this invention has been filed earlier than the following in any country foreign to the United States prior to this application by me or my legal representatives or assigns:

German Application No. 198 15 874.2, filed April 8, 1998, the International Priority of which is claimed under 35 U.S.C. §119 and International Application No. PCT/DE99/00901, filed March 25, 1999, the Priority of which is claimed under 35 U.S.C. §120.

I hereby appoint the following attorneys and/or agents to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

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I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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